

REMARKS

Applicant respectfully requests the reconsideration of this application and the consideration of the following remarks.

The Examiner asserted that

"To establish long felt need, Applicant must supply evidence to prove this statement and argument with an Affidavit under 37 CFR 1.132." (Page 11, lines 3-4, Office Action mailed July 26, 2005)

Applicant respectfully disagrees. 37 CFR 1.132 provides:

"When any claim of an application or a patent under reexamination is rejected or objected to, any evidence submitted to traverse the rejection or objection on a basis *not otherwise provided for* must be by way of an oath or declaration under this section." (37 CFR 1.132)

Although any evidence submitted to traverse the rejection or objection on a basis *not otherwise provided for* must be by way of an oath or declaration under this section, the evidence used for the argument has been *otherwise provided for*. Specifically, the long felt need is established based upon the references and reasoning provided by the Examiner. Thus, no Affidavit under 37 CFR 1.132 is necessary.

Specifically, the references and at least some of the reasoning provided the Examiner to establish the obviousness are used to establish "the long felt need", which contradicts the conclusion of obviousness. The Examiner relied upon the cited references to establish the need/motivation. If this reasoning of the Examiner were proper, the age of the references would further establish the element of "long felt". Thus, "the long felt need" is based on the evidence already provided by the Examiner. No Affidavit under 37 CFR 1.132 is necessary.

Note that "the long felt need" is based on the Examiner's reasoning. "The long felt need" might not be established, if the Examiner were wrong with respect to the need/motivation. However, if the Examiner were wrong with respect to the need/motivation, the Examiner's obviousness conclusion would then be also wrong. Thus, when the evidence provided by the Examiner is considered as a whole, the conclusion of non-obviousness should be made.

Further, in view of the Examiner's reasoning to combine, it is clear that references tried but failed provide the invention as claimed. For example, in view of "the long felt need" given in Mennemeier (established based on the Examiner's reasoning), Chehراzi tried to design a single instruction but failed to reach the invention as claimed. Thus, the logical conclusion is non-obviousness.

Claim 41 was rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Applicant respectfully disagrees. The Office Action asserted that "The specification has not disclosed how a memory controller is not on the integrated circuit with a processor while the processor is on the integrated circuit with the memory controller." Applicant respectfully submits that this assertion is not relevant to claim 41. Claim 41 depends from claim 40 which further depends from claim 23. Claim 23 recites "the microprocessor is *a media processor disposed on an integrated circuit* with a memory controller". Claim 41 further recites "the memory controller is usable by *a central processing unit (CPU) not disposed on the integrated circuit* to access the memory". The assertion of the Office Action involves only a single processor, while claim 41 involves "*a central processing unit (CPU)*" and "*a media processor*". There is no indication in the claim that they are the same processor. For example, Figure 5B shows a media processor (1510) with memory controller (1516), which is separate from the host processor(s) (1511). For example, Figure 4B of the present invention shows a media processor (1413) on the system

core logic (1410) and separate one or more host processors (1411) that are not on the system core logic (1410).

Therefore, the rejection under 35 U.S.C. 112, first paragraph, is based on the improper interpretation of the claim (e.g., erroneously considering *a central processing unit (CPU)* as a processor and considering *a media processor* as the same processor). Thus, the withdrawal of the rejection is respectfully requested.

Claims 1-3, 5-7, 9-14, 16-18, 20-28, 30-32, 34-39 and 40 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,282,556 (hereinafter "Chehrazi") in view of U.S. Patent No. 6,036,350 (hereinafter "Mennemeier").

To make the rejection under 35 U.S.C. 103(a), the Office Action took the position to ignore the instructions used in Mennemeier and take only the fact that a vector of absolute differences is outputted to a register file, even though Mennemeier uses multiple instructions to compute a vector of absolute differences. Thus, the Examiner established the need to output a vector of absolute differences to a register file based on Mennemeier. Based on the consideration that Mennemeier outputs a vector of absolute differences to a register file while ignoring how the vector of absolute differences is computed in Mennemeier, the Office Action asserted that it would be obvious to modify Chehrazi to make a new instruction as recited in the pending claims.

Thus, the reasoning of the Office Action established the "need." The actual date of Mennemeier establishes that, if there were such a need as suggested by the Office Action, the need would be long felt (four years before Chehrazi and six years before the present application).

Mennemeier is a continuation of an application that was filed in 1995. Therefore, the need to output a vector of absolute differences to a register file in a way as described in Mennemeier would have been known since 1995. The Office Action took the position that

such a prior art reference would motivate one to change the SABD instruction of Chehrazi in a way suggested in the Office Action. However, such a position is not consistent with the fact that four (4) years after Mennemeier, Chehrazi failed to disclose the instruction suggested in the Office Action. Chehrazi was filed in 1999, which was four years after Mennemeier. Chehrazi tried to make a single instruction but failed to reach the instruction as claimed. Thus, the absence of an instruction as recited in the pending claims from Chehrazi is a clear indication of non-obviousness.

Furthermore, the present application was filed in 2001. The absence of a reference showing an instruction as cited in the pending claims during the long period of time since 1995 is a clear indication of non-obviousness.

Thus, applicant respectfully submits that, when the cited references are viewed as a whole, the subject matter as recited in the pending claims is not obvious.

The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness under 35 U.S.C. 103. A *prima facie* case of obviousness is established by presenting evidence that would have led one of ordinary skill in the art to combine the relevant teachings of the references to arrive at the claimed invention. It is impermissible to simply make a hindsight reconstruction of the claimed invention using the claim as a template and filling the gaps using the elements from the references.

The evidence and reasoning provided by the examiner for the rejection actually provides the indication of non-obviousness. Thus, the obviousness conclusion is based on the impermissible knowledge gleaned from the applicant's disclosure.

Applicant respectfully submits that the interpretation of the term "memory controller" in the Office Action is improper. The Office Action asserted that

"This suggests that there is a control unit that controls data and instructions that are fetched from memory. Thus, the control unit is a memory

controller that controls when data and instructions are fetched from memory”

(Page 13, Item 46, Office Action mailed July 26, 2005)

Applicant respectfully submits that such reasoning is erroneous. For example, a microprocessor as a CPU may control data and instructions that are fetched from memory; a bus may control data and instructions that are fetched from memory; a remote palm top computer may control data and instructions that are fetched from memory through a communication network. If the reasoning of the Office Action were followed, microprocessors, buses and remote palm top computers would be all memory controllers, which is clearly improper and unreasonable. Applicant respectfully requests reasonable interpretation of terms.

Claims 4, 15, 29 and 39 were rejection under 35 U.S.C. 103(a) as being unpatentable over Chehrazi in view of Mennemeier and further in view of European Patent Application Publication No. 0,485,833 A2 (hereinafter “Diefendorff”).

The Office Action used Diefendorff to establish the need/motivation (see, e.g., page 10, item 36, Office Action mailed July 26, 2005. Since Diefendorff was published in 1992 (seven years before Chehrazi and nine years before the present application), the element of “long felt” of “the long felt need” is established based on the Examiner’s assertion and the date of Diefendorff. Thus, the Examiner provided the evidence to establish “the long felt need” in the rejection. No Affidavit under 37 CFR 1.132 is necessary. The “long felt need” indicates the non-obviousness.

When the references are viewed together, it is clear that the combination suggested by the Office Action is based on the disclosure of Applicant’s disclosure, not based on the references. The combination suggested by the Office Action is clearly constructed using the claims as the template. The combination is not based on the references alone.

Applicant respectfully submits that the pending claims are patentable over the cited references.

For example, claim 1 recites:

1. (Previously Presented) A method for execution by a microprocessor in response to receiving a single instruction, the method comprising:
receiving a first plurality of numbers and a second plurality of numbers; and
generating a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers;
wherein the third plurality of numbers are saved in an entry in a register file;
wherein the above operations are performed in response to the microprocessor receiving the single instruction.

Chehrazi (e.g., Col. 20, line 42 – Col. 21, line 12) shows the sum of absolute differences (SABD) instruction. Figure 20B of Chehrazi clearly shows that the SABD instruction outputs the sum, not the vector of absolute differences. The SABD instruction as illustrated in Figure 20A shows two input registers (Vt and Vs) and only one destination register (Vd) (see also, Col. 20, lines 56-58, Chehrazi). Thus, no single instruction of Chehrazi computes a vector of absolute differences and outputs the vector of absolute differences in an entry of a register file.

Mennemeier shows a four-instruction execution process to compute the absolute differences (see, e.g., Col. 5, lines 9-10 and Figure 3 of Mennemeier), which uses a Packed Comparison For Greater Than Word (PCMPGTW) instruction, a Packed Exclusive-OR (PXOR) instruction, a Packed AND (PAND) instruction, and a Packed Subtraction (PSUBW) instruction. Thus, Mennemeier uses an instruction set which is very different from Chehrazi.

When viewed together, Chehrazi and Mennemeier show no indication of an arrangement in which a single instruction is used to compute and output absolute differences. The fact that Chehrazi shows a sum of absolute differences instruction that does not output absolute differences is a clear indication of non-obviousness. No Affidavit under 37 CFR 1.132 is necessary.

As discussed above, the modification of Chehrazi in a way as suggested in the Office Action in view of Mennemeier is not obvious, because of the absence of an actual such modification in the long period of time before the filing of the present application and after Mennemeier. Applicant respectfully submits that the modification of Chehrazi suggested in the Office Action is a hindsight reconstruction using the pending claim as the template and the filling the gaps using the elements from Chehrazi and Mennemeier. Such modification does not come naturally from the description of Chehrazi and Mennemeier.

Claims 12 and 26 recite limitations similar to that discussed above. Thus, claims 1, 12 and 26 and their dependent claims are patentable over Chehrazi and Mennemeier.

Further, for example, claim 23 recites:

23. (Previously Presented) An execution unit in a microprocessor, the execution unit comprising:
 - a first circuit configured to receive a first plurality of numbers;
 - a second circuit configured to receive a second plurality of numbers;
 - and
 - a third circuit coupled to the first circuit and the second circuit, the third circuit, in response to the microprocessor receiving a single instruction, generating a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers

wherein the microprocessor is a media processor disposed on an integrated circuit with a memory controller.

The rejection of claim 23 was based on the improper interpretation of the terms "memory controller", "CPU" and "processor", as discussed above. The position of "memory controllers are an inherent part of a processor" is improper.

Since neither Chehrazi nor Mennemeier shows the limitation of "a media processor disposed on an integrated circuit with a memory controller", claims 2 and 23 and their dependent claims are patentable over the cited references.

Further, for example, claim 37 recites:

37. (Previously Presented) A method as in claim 1, wherein a type of each of the first and second pluralities of numbers is floating point number.

In rejecting claim 37, the Office Action misapplied the elements of Chehrazi, based on the description about the MADD instruction (Col. 9, lines 37-41, Chehrazi) which is clearly not the SABD instruction and/or based on speculation in view of Col. 1, lines 19-21, Chehrazi. The rejection for claim 37 is improper.

Further, for example, claim 38 recites:

38. (Previously Presented) A media as in claim 12, wherein the microprocessor is a media processor disposed with a memory controller on an integrated circuit.

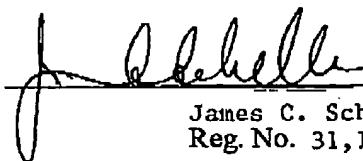
Apparently, the rejection for claim 38 was based on the improper interpretation of the definition for central processing unit (CPU).

Please charge any shortages or credit any overages to Deposit Account No. 02-2666. Furthermore, if an extension is required, Applicant hereby requests such extension.

Respectfully submitted,

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